ADJUSTING DIE PLACEMENT ON A SEMICONDUCTOR WAFER TO INCREASE YIELD

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the benefit of U.S. Provisional Application No. 60/454,706, titled A PROCESS FOR IMPROVING CYCLE TIME TO ACHIEVE MAXIMUM YIELD OF SEMICONDUCTOR CHIPS, filed March 17, 2003, the entire content of which is incorporated herein by reference.

BACKGROUND

1. Field of the Invention

[0002] The present application relates to die placement on a semiconductor wafer, and more particularly to adjusting a die placement to increase yield of the dice formed on the wafer.

2. Related Art

[0003] Semiconductor devices are typically manufactured by fabricating the devices on a semiconductor wafer. An individual device is formed as a die on the wafer using known semiconductor fabrication processes. Depending on the size of the die, a single wafer can contain hundreds of dice. The dice are generally arranged in a pattern (i.e., a die placement) on the wafer to maximize the number of dice on the wafer.

[0004] During a fabrication process, a processing structure can contact the wafer or emit a substance that contacts the wafer. Dice that are formed in, adjacent, or opposite locations on the wafer that come in contact with the processing structure or the substance emitted by the processing structure are typically bad, meaning that the devices on the dice have unacceptable failure rates or do not function at all. Thus, the overall yield, meaning the total number of good dice formed on the wafer, is reduced.

[0005] In one approach to increase yield, the processing structure is moved to adjust the location on the wafer that is contacted by the processing structure or the substance emitted by the processing structure. There are, however, only a limited number of locations where the

processing structure can be moved. Additionally, the increase in yield is typically small, particularly relative to the time and cost associated with moving the processing structure.

SUMMARY

[0006] In one exemplary embodiment, a die placement of dice to be formed on a wafer is adjusted by obtaining a die placement and one or more locations on the wafer contacted by one or more processing structures or a substance emitted by one or more processing structures. The die placement is adjusted based on the obtained one or more locations on the wafer.

DESCRIPTION OF DRAWING FIGURES

[0007] The present application can be best understood by reference to the following description taken in conjunction with the accompanying drawing figures, in which like parts may be referred to by like numerals:

[0008] Fig. 1 depicts an exemplary die placement of dice to be formed on a semiconductor wafer with locations on the wafer contacted by processing structures or a substance emitted by processing structures;

[0009] Fig. 2 depicts the exemplary die placement depicted in Fig. 1 with different locations on the wafer contacted by processing structures or a substance emitted by processing structures;

[0010] Fig. 3 depicts an exemplary process of adjusting a die placement;

[0011] Fig. 4 depicts an exemplary process of selecting a die placement during the exemplary process depicted in Fig. 3;

[0012] Fig. 5 depicts an exemplary die placement of dice to be formed on a semiconductor wafer with locations on the wafer contacted by processing structures or a substance emitted by processing structures;

[0013] Fig. 6 depicts another exemplary process of adjusting a die placement;

[0014] Fig. 7 depicts another exemplary process of selecting a die placement during the exemplary process depicted in Fig. 6; and

[0015] Fig. 8 depicts an exemplary die placement and locations on the wafer contacted by processing structures or a substance emitted by processing structures.

DETAILED DESCRIPTION

[0016] The following description sets forth numerous specific configurations, parameters, and the like. It should be recognized, however, that such description is not intended as a limitation on the scope of the present invention, but is instead provided as a description of exemplary embodiments.

[0017] With reference to Fig. 1, an exemplary semiconductor wafer 102 is depicted having a center 104 and locations 106, 108 on wafer 102 contacted by processing structures or a substance emitted by processing structures. For example, the processing structures can include a clamp that contacts the wafer, a jet that emits a chemical solution or water that contacts the wafer, and the like. It should be recognized that the size, number, and positions of locations 106, 108 can vary depending on the processing structures and the fabrication process used. For example, there can be one location on wafer 102 contacted by a single processing structure.

[0018] Fig. 1 also depicts a die placement 110 of a plurality of reticle arrays 112. In one exemplary embodiment, each reticle array 112 includes a plurality of dice arranged in an array, such as 25 dice arranged in a 5x5 array. It should be recognized, however, that a reticle array 112 can include any number of dice arranged in various patterns. Additionally, it should be recognized that die placement 110 can include any number of reticle arrays 112 arranged in various patterns.

[0019] In Fig. 1, locations 106, 108 are depicted as being on the same surface on wafer 102 as the surface on which dice are to be formed. It should be recognized, however, that locations 106, 108 can be on the opposite surface of wafer 102 as the surface on which dice are to be formed. For example, dice can be formed on a front side of wafer 102, and a clamp can contact a location on the back side of the wafer opposite the front side.

[0020] In one simulation, a die placement 110 as depicted in Fig. 1 was used. In the simulation, a reticle array 112 of 25 dice arranged in a 5x5 array was used. Additionally, clamps

were assumed to be located to contact wafer 102 in locations 106, 108 as depicted in Fig. 1. The total yield resulting from this simulation was 1953 yielding (good) dice.

[0021] With reference to Fig. 2, locations 106, 108 can be adjusted to increase yield. More particularly, Fig. 2 depicts exemplary relocation areas 202 and 204 defined by boundary lines 206 and 208. It should be recognized, however, that the sizes, shapes and locations of relocation areas 202, 204 can vary depending on the on the processing structures and the fabrication process used.

[0022] In one simulation, the clamps were assumed to have been moved to contact locations 106, 108 as depicted in Fig. 2. Die placement 110 and reticle arrays 112 were kept the same as in the simulation described above in connection with Fig. 1. The total yield resulting from this simulation was 1956 yielding (good) dice. Thus, the increase in yield from the simulation described above in connection with Fig. 1 was three yielding (good) dice.

[0023] With reference to Fig. 3, an exemplary process 300 is depicted of adjusting a die placement of dice to be formed on a wafer. In step 302, a die placement of dice to be formed on the wafer is obtained. For example, with reference to Fig. 1, assume that die placement 110 in Fig. 1 represents an initial die placement that is obtained. As noted above, die placement 110 can include any number of reticle arrays 112 arranged in various patterns, and each reticle array 112 can include any number of dice arranged in various patterns.

[0024] With reference again to Fig. 3, in step 304, one or more locations on the wafer contacted by one or more processing structures or a substance emitted by one or more processing structures are obtained. For example, with reference to Fig. 1, assume that locations 106, 108 in Fig. 1 represent initial locations on wafer 102 contacted by the processing structures or the substance emitted by the processing structures.

[0025] With reference to Fig. 3, in step 306, the die placement is adjusted based on the obtained one or more locations on the wafer. In one exemplary embodiment, the die placement is adjusted to increase yield of the dice formed on the wafer. In particular, the die placement is adjusted to reduce the number of bad dice associated with the one or more locations on the wafer.

[0026] For example, in one simulation, die placement 110 in Fig. 1 was adjusted to die placement 502 in Fig. 5, while locations 106, 108 remained the same. The total yield resulting from this simulation was 1963 yielding (good) dice. Thus, the increase in yield from the simulation described above in connection with Fig. 2 was seven more yielding (good) dice, and the increase in yield from the simulation described above in connection with Fig. 1 was 10 more yielding (good) dice.

[0027] With reference to Fig. 4, an exemplary process 400 is depicted of selecting a die placement. In step 402, a plurality of die placements having different arrangements of reticle arrays, and thus different arrangements of dice, are generated. In step 404, a yield associated with each of the plurality of die placements is determined. In step 406, the die placement with the highest yield is selected.

[0028] Process 400 can be performed as a batch process. More particularly, the plurality of die placements are generated together, then the yields for the plurality of die placements are generated together.

[0029] Alternatively, process 400 can be performed iteratively. More particularly, a first die placement can be generated, then the yield for the first die placement is determined. After the yield is determined, a second die placement is generated, then the yield for the second die placement is determined.

[0030] With reference to Fig. 6, an exemplary process 600 is depicted of adjusting a die placement of dice to be formed on a wafer. In step 602, a die placement of dice to be formed on the wafer is obtained. In step 604, one or more locations on the wafer contacted by one or more processing structures or a substance emitted by one or more processing structures are obtained. In step 606, the die placement is adjusted based on the obtained one or more locations on the wafer. In step 608, the one or more locations on the wafer are adjusted based on the die placement.

[0031] In process 600, the die placement and the one or more locations on the wafer are adjusted together. In one exemplary embodiment, the die placement and the one or more locations on the wafer are adjusted to increase yield of the dice formed on the wafer. In

particular, the die placement and the one or more locations on the wafer are adjusted to reduce the number of bad dice associated with the one or more locations on the wafer.

[0032] For example, in one simulation, die placement 110 in Fig. 1 was adjusted to die placement 802 in Fig. 8, and locations 106, 108 were adjusted to new locations as depicted in Fig. 8. The total yield resulting from this simulation was 1967 yielding (good) dice. Thus, the increase in yield from the simulation described above in connection with Fig. 5 was four more yielding (good) dice, the increase in yield from the simulation described above in connection with Fig. 2 was 11 more yielding (good) dice, and the increase in yield from the simulation described above in connection with Fig. 1 was 14 more yielding (good) dice.

[0033] With reference to Fig. 7, an exemplary process 700 is depicted of selecting a die placement and one or more locations on the wafer. In step 702, a plurality of combinations of die placement and one or more locations on the wafer are generated. In step 704, a yield associated with each combination of die placement and one or more locations on the wafer is determined. In step 706, the combination of die placement and one or more locations on the wafer with the highest yield is selected.

[0034] Process 700 can be performed as a batch process. More particularly, the plurality of combinations of die placement and locations of one or more processing structures are generated together, then the yields for the combinations of die placement and locations of one or more processing structures are generated together.

[0035] Alternatively, process 700 can be performed iteratively. More particularly, a first combination of die placement and one or more locations on the wafer can be generated, then the yield for the first combination of die placement and one or more locations on the wafer is determined. After the yield is determined, a second combination of die placement and one or more locations on the wafer is generated, then the yield for the second combination of die placement and one or more locations on the wafer is determined.

[0036] Although exemplary embodiments have been described, various modifications can be made without departing from the spirit and/or scope of the present invention. Therefore, the present invention should not be construed as being limited to the specific forms shown in the drawings and described above.